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**Analog Generator  
for Real-Time Display  
of Curves**

28 July 1965

Prepared under Electronic Systems Division Contract AF 19(628)-5167 by

**Lincoln Laboratory**

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Lexington, Massachusetts

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MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
LINCOLN LABORATORY

ANALOG GENERATOR FOR REAL-TIME DISPLAY OF CURVES

*T. E. JOHNSON*

*Group 23*

TECHNICAL REPORT 398

28 JULY 1965

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## ABSTRACT

This report discusses the design and performance of a low-cost analog generator capable of forming rotated cubics and conics for real-time display on a cathode-ray tube. Use of high-bandwidth operational amplifiers and field-effect transistors in the analog switches allows fast and accurate operation.

Accepted for the Air Force  
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Lt Colonel, USAF  
Chief, Lincoln Laboratory Office

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## ANALOG GENERATOR FOR REAL-TIME DISPLAY OF CURVES

### I. INTRODUCTION

Real-time interaction between man and digital computers often requires a computer-directed graphical display. The cathode-ray tube (CRT) has so far been the only candidate for applications requiring fast write and erase times. However, in addition to an adequate display surface, there is need for more advanced generators which are capable of drawing straight lines and curves without demanding constant attention from the computer. Although digital techniques required to draw curves and straight lines without performing point-by-point calculation by the computer are well known, the expense and complexity of these digital display generators have discouraged construction of useful devices. Analog methods for generating curves are simpler and more direct, but have found little use because of speed and accuracy limitations and the high price of analog switching components.

Two recent advances in solid-state analog devices that have changed this situation are the high-current field-effect transistor (FET) and the high-bandwidth, high-power operational amplifier. The operational amplifier (which costs about \$100) is half the size of a cigarette pack, operates at  $\pm 10$  volts and  $\pm 20$  ma, and has a 100-Mcps gain-bandwidth product.

The advent of the high-current FET provides, for the first time, analog switching speeds in the microsecond region with no current or voltage offset. Because of its high current range, the FET can switch bipolar currents up to 2 ma at constant impedance.

This report discusses the design and performance of a low-cost analog generator capable of forming rotated cubics and conics for display. The generator, presently in operation on the TX-2 computer at Lincoln Laboratory, has an accuracy of 0.1 percent and is capable of producing over 3000 arbitrary curves per second.

The analog generator presented in this report should be regarded as an extremely fast general-purpose analog computer that has been adapted for the particular application of real-time display. The analog computer is driven by a general-purpose digital computer that supplies the parameters, selects the computing paths, and furnishes the length of time the analog generator must run to form any one solution (the display of a curve). While the analog generator is computing the locus of the curve, the driving digital computer is disconnected from the generator and is free for general computation. Upon completion of a curve, the generator will interrupt the digital computer, requesting more information for the next curve which is supplied within a few instruction cycles. Thus, the computational load on the digital computer necessary to initiate and maintain a complicated display of cubics and conics is greatly reduced. After all the curves of a drawing have been displayed, the digital computer must cycle through all the curves repeatedly to maintain the display on the CRT face.

For most applications, where one is merely inspecting a drawing for content and topology and not taking dimensions off with a pair of dividers, the 0.1-percent accuracy of an analog curve drawing generator is entirely sufficient.

## II. DISPLAY GENERATION

The analog computation methods used in generating the voltage signals for display are based on standard techniques. Different combinations of integration and multiplication are used to form the various curve functions. The digital computer that drives the generator supplies mode information, which is decoded at the analog generator into switching signals. These commands are used to select the various computing paths available by closing the appropriate analog switch.

Curves seen on the scope in X- (horizontal) and Y- (vertical) coordinates are actually cross-plots of two parametric equations in time. This is necessary, of course, because electronic analog integration is most easily accomplished in the time domain. Parametric representations allow (among other things) the display of infinite slopes merely by holding the horizontal deflection voltage constant and by varying the vertical axis. Therefore, the analog generator is composed of two sets of curve generators – one for each axis. To draw a line, for example, the generator must form two simultaneous linear voltages:  $X = C_x t + D_x$ , and  $Y = C_y t + D_y$  (where  $t$  is time,  $0 \leq t \leq T$ , and  $T$  is the final value); these voltages cross-plot on the scope as  $Y = (C_y/C_x)(X) + [D_y - (C_y/C_x)D_x] = mX + K$ . In the following discussion on computation methods, it should be kept in mind that computing elements must be duplicated to provide for both coordinates. The duration of computation time ( $t$  in the parametric equation) is controlled by an internal interval timer that is loaded by the driving digital computer. The particular digital computer (TX-2) used to run the analog generator has 36-bit words available. Thus, loading commands have room for parallel loading of  $x$  and  $y$  arguments of ten bits each, and a code field for mode specification (i.e., to identify the arguments).

### A. Points

$$X = D_x$$

$$Y = D_y$$

An initial voltage is placed over the position integrator and displayed. The generator stores this analog position for subsequent use as an initial point for a curve, if desired.

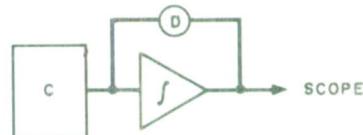
Computer loading instructions:

LOAD ( $D_x$ ,  $D_y$ , DP)    DP = code word for display point

### B. Lines

$$X = C_x t + D_x$$

$$Y = C_y t + D_y$$



A constant current equal to  $C$  is integrated once, beginning with the initial condition  $D$  over the integrator. The terminal computed voltage position is stored;  $C$  is not stored when the line is terminated by expiration of the interval timer.

Computer loading instructions:

LOAD ( $D_x$ ,  $D_y$ , LP)      LP = load start point (not necessary if curve uses previous position, i.e., when one curve begins where the previous curve terminates)

LOAD (T, LT)      LT = load time

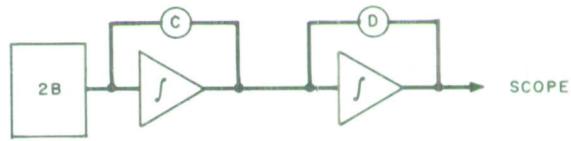
LOAD ( $C_x$ ,  $C_y$ , EL)      EL = execute line

Note that the C's represent parametric rates whose ratio  $C_y/C_x$  represents slopes. Integration of rates, rather than the simpler full discharge of a linearly cross-plotting RC network, is used to form the line plot so an over-all saving can be gained by using the same integrator in higher order curve formation. Rates must be used in higher order curves. Since the lines are generated by integration, the intensity of the line is constant throughout the length of the displayed line (CRT beam sweep is constant). A line cannot be specified to the generator by supplying its end points. The length of the line equals rate times time.

### C. Parabolas

$$X = B_x t^2 + C_x t + D_x$$

$$Y = B_y t^2 + C_y t + D_y$$



A constant current equal to  $2B$  is integrated twice, beginning with the rate  $C$  and the start point  $D$  as initial conditions over the integrators. The terminal rate and position voltages are stored for use as initial conditions for a subsequent conic or cubic. The rate is not available for a subsequent line unless the line is a parabola with  $B = 0$ . When lines are drawn using the execute line (EL) mode, the rate integrator is switched out of the computing path obliterating its stored information. Rotated parabolas are drawn by properly choosing  $B$  and  $C$ . Intensity variation is parabolic, but usually never varies by more than a factor of two.

Computer loading instructions:

LOAD ( $D_x$ ,  $D_y$ , LP)      LP = load start point (not necessary if curve uses previous position)

LOAD ( $C_x$ ,  $C_y$ , LR)      LR = load start rate (not necessary if curve uses previous rate)

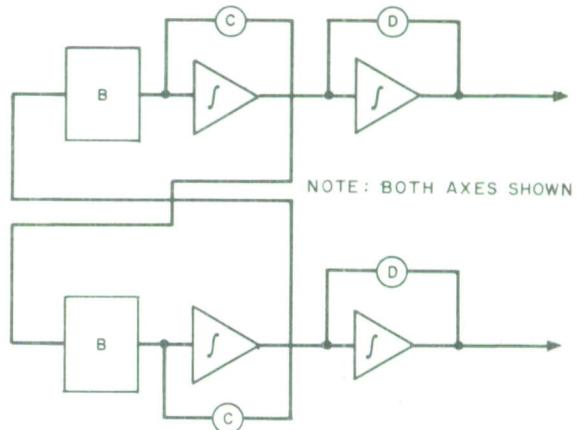
LOAD (T, LT)      LT = load time

LOAD ( $2B_x$ ,  $2B_y$ , EP)      EP = execute parabola

### D. Circles (and Hyperbolas)

$$X = \frac{C_x}{B} \sin Bt + D_x$$

$$Y = \frac{C_y}{B} (1 - \cos Bt) + D_y$$



Instead of beginning with the integration of a constant current, a current proportional to B times the output of the opposite rate integrator is integrated. The feedback loop forms a sine-cosine generator whose outputs are of a constant amplitude C, and oscillate at a frequency proportional to B. These outputs are integrated once more to form the deflection drive. This method offers circles whose angular velocity times radius is constant over all radii. This means that the tangential velocity of the beam is constant, giving a constant intensity display for all circles. Furthermore, the additional integration of the sine-cosine generator output allows circles whose centers are not necessarily on the scope face. This would not be possible with a normal second-order sine-cosine generator, since overflow would occur. Note then, the D initial conditions specify the start point of a circle arc, not the center of the circle. One of the B's ( $B_x$  or  $B_y$ ) must be negative to provide the necessary negative feedback for oscillation. The multiplier is a four-quadrant device which performs the inversion. If  $B_x$  and  $B_y$  are both positive, orthogonal hyperbolas result. As in the case of parabolas, the terminal rate and position voltage are stored. Circles can be made to wind in either direction by properly choosing the coefficients.

Computer loading instructions:

LOAD ( $D_x$ ,  $D_y$ , LP)

LP = load start point (not necessary if curve uses previous position)

LOAD ( $C_x$ ,  $C_y$ , LR)

LR = load start rate (not necessary if curve uses previous rate)

LOAD (T, LT)

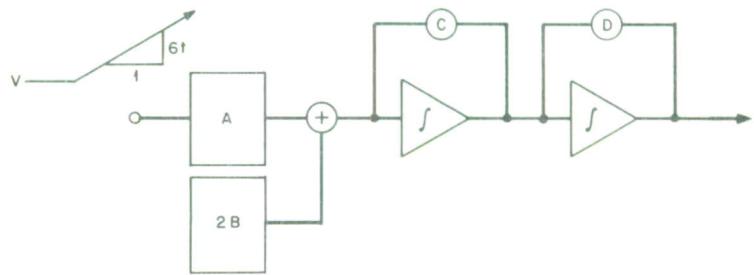
LT = load time

LOAD ( $B_x$ ,  $B_y$ , EC)

EC = execute circle

### E. Polynomial Cubics

$$X = A_x t^3 + B_x t^2 + C_x t + D_x$$



$$Y = A_y t^3 + B_y t^2 + C_y t + D_y$$

An externally formed precision ramp, proportional to  $6t$ , is multiplied by A and added to a constant current  $2B$ . This sum is integrated over the initial rate C and initial position D. The terminal rate and position are saved. The technique of combined multiplication-integration rather than total integration was used to overcome the accuracy limitations of triple integration. Furthermore, overflow of the second derivative term  $6At + 2B$  is not possible as it would be by using a third integrator, simply because there is no integrator to saturate.

Computer loading instructions:

LOAD ( $D_x$ ,  $D_y$ , LP)

LP = load start point (not necessary if curve uses previous position)

LOAD ( $C_x$ ,  $C_y$ , LR)

LR = load start rate (not necessary if curve uses previous rate)

LOAD (T, LT)

LT = load time

LOAD ( $B_x$ ,  $B_y$ , L2D)

L2D = load second derivative

LOAD ( $A_x$ ,  $A_y$ , EQ)

EQ = execute cubic

The composite assembly of all the available computing paths as they appear in the generator is shown in Fig. 1.

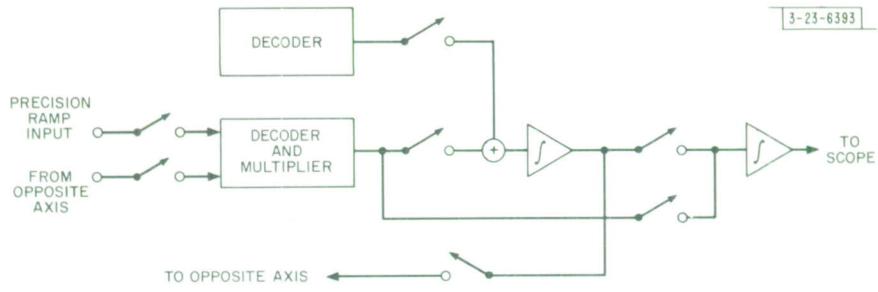


Fig. 1. Available computing paths.

### III. DIGITAL-TO-ANALOG CONVERSION, MULTIPLICATION AND LOADING

#### A. Decoding and Multiplication

During curve computation, a constant current proportional to a digital number is integrated successively to form the display. This current is supplied by a combination multiplier and digital-to-analog (D-A) decoder. The decoder is designed to convert 10-bit, ones-complement numbers. Each bit of the incoming binary number gates an analog switch. If the bit is a 1, the switch is closed, passing a current proportional to the bit value into the summing amplifier (shown in Fig. 2). The sign bit is complemented before gating; the sum of the switched currents is biased by a positive current equal to 1, giving a bipolar output at the summing amplifier. Figure 3 shows how the output varies with the digital input. The first operational amplifier serves to invert the reference voltage for biasing purposes. The assembly can be viewed as a digitally set potentiometer with a bias. Current used for integration is formed by dropping the summing output voltage across an integrator input resistor. The D-A decoder design (Fig. 2) can be converted to a four-quadrant multiplier by regarding the reference voltage as a variable. Figure 4 shows the reference voltage switched out and a variable input switched in, as it is in the generator. The multiplier forms an analog output from an analog and a digital input. Four-quadrant multiplication is possible because the bias varies, changing sign when the input changes sign.

Because the D-A converter acts as a multiplier, bipolar voltages are switched at the variable resistor necessitating the use of analog switches. A resistor ladder network is not used for D-A decoding because bipolar operation is difficult.

#### B. Loading

All displayed curves require initial condition voltages to be placed over program-selected integrators. This is accomplished by charging the feedback capacitor of the selected integrator as shown in Fig. 5. The digital number specifying the initial condition value is decoded into a reference current ( $i_{ref}$ ) which is compared with a current proportional to the present voltage at the integrator output. The difference appears at the summing amplifier as a voltage  $V_{sum}$ ; this voltage is placed across the input resistor of the integrator, dumping current equal to  $V_{sum}/r$  into the capacitor. The current is removed from the output side of the capacitor by the operational amplifier, causing the capacitor to charge and change its voltage. This voltage is fed back to the summing amplifier for comparison. The final charge  $V_o$  is proportional to  $i_{ref}$ ; it is reached exponentially as shown by Eq. (2) in Fig. 5. Charge time is controlled by the time constant  $rC$  (the integrator feedback capacitor and the integrator input resistance). The choice of  $rC$  values is, in turn, affected by other considerations. The capacitor cannot be made too small, or storage of the initial condition will be difficult; the resistor cannot be too small, otherwise it will draw more

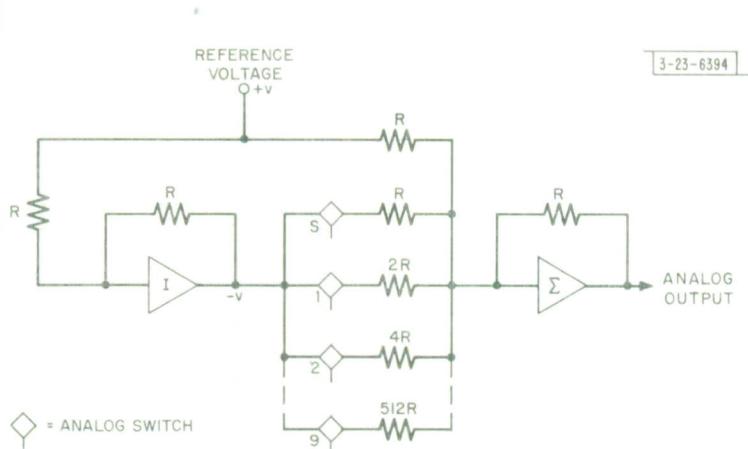


Fig. 2. D-A decoding circuitry.

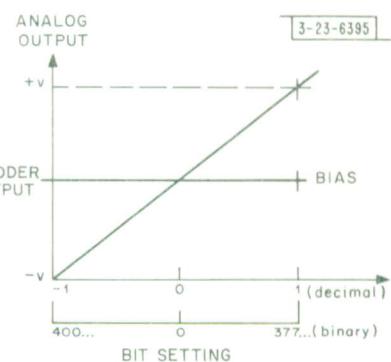


Fig. 3. Bipolar D-A decoding.

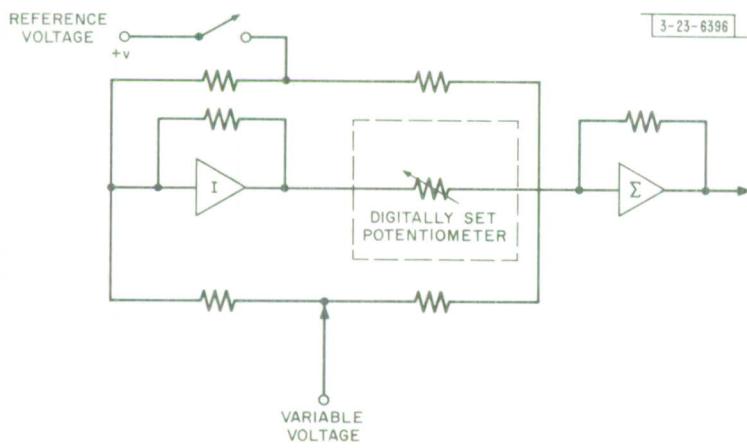
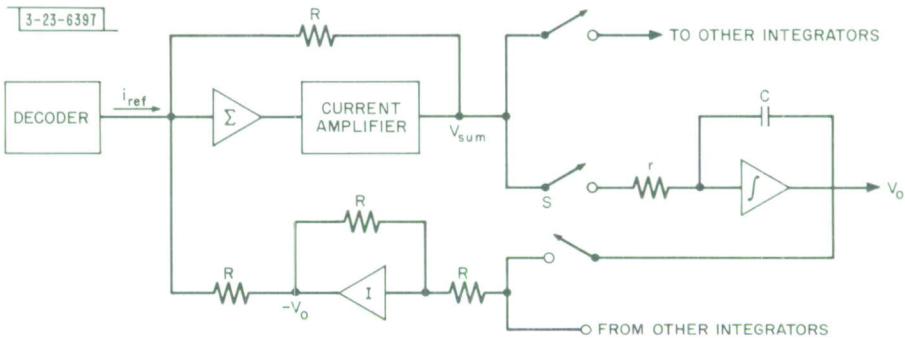


Fig. 4. Multiplier circuitry.



From analog computing theory,

$$\frac{dV_o}{dt} = -\frac{V_{sum}}{rC}$$

$$V_{sum} = -(i_{ref}R - V_o) \quad .$$

Combining

$$\frac{dV_o}{dt} + \frac{V_o}{rC} = \frac{i_{ref}R}{rC} \quad . \quad (1)$$

Solving Eq.(1) for  $V_o$ ,

$$V_o = i_{ref}R[1 - e^{-(t/rC)}] \quad . \quad (2)$$

Steady-state solution

$$V_o = i_{ref}R \quad .$$

Fig. 5. Initial condition loading circuits and governing equations.

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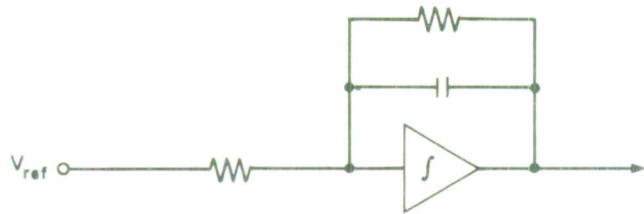


Fig. 6. Alternative charging method.

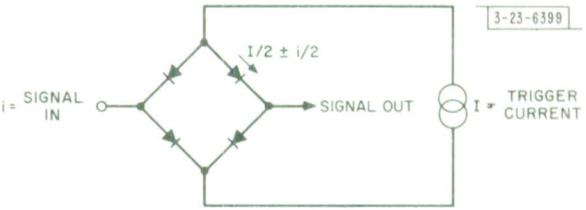
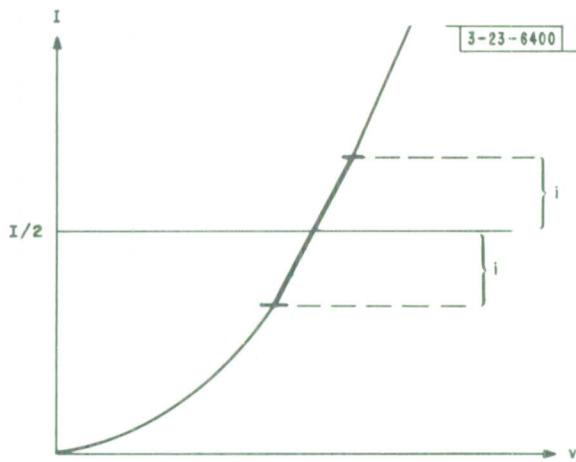
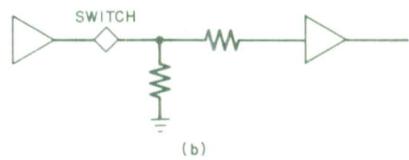
Fig. 7. (a) Diode bridge analog switch;  
(b) environment.

Fig. 8. Operating range of diode bridge elements.

current than is available causing the system to oscillate. By putting a current amplifier in the feedback loop of the summing amplifier to allow a small  $r$ , the time required to charge an integrator to within 0.1 percent of the input value is 25  $\mu$ sec. Charging by feedback was used because the analog switches exhibit "on"-resistance of 50 to 100 ohms, as compared to relay contact resistances of fractions of milliohms. With relays, the integrator capacitor is normally switched to ground from the summing point side; the capacitor is then charged from the output of the integrator amplifier. (If this technique is used with solid-state switches, the "on"-resistance in the capacitor feedback back path will degrade the output.)

Another alternative is to leave the integrator capacitor connected permanently as it is in the analog generator, but to charge from the output of the integrator amplifier under control of a feedback resistor (Fig. 6). The difficulty with this scheme is that, in order to achieve fast charging times, the feedback resistance has to pass large continuous currents through the solid-state switch even during steady state. At large currents, the switch resistance begins to change drastically relative to the feedback resistor affecting the gain of the loop, resulting in a nonlinear charge depending on the value of  $V_{ref}$ . This high current persists at the end of the charge because of the output voltage drop through the feedback.

In the scheme adopted for the analog generator, at steady state no current passes through switch S or resistance  $r$  (Fig. 5) since  $V_{sum}$  goes to zero. Even though the switch does pass high current at the beginning of the charge time and the resistance becomes nonlinear, no signal deterioration occurs since the integrator input resistor only determines the charging time constant and not the final charge value.

The analog generator charges the appropriate integrator by decoding the load instruction from the driving digital computer into the switching signals that close the corresponding analog switches. Matching X- and Y-axis integrators are charged in parallel. Charging is terminated by the expiration of a timer. The digital computer is not connected during the load time, so it is available for use during this period.

#### IV. DC SWITCHING

The solid-state analog switch represents the keystone to successful application of analog techniques to the display generator problem. Normally, it is here that most signal deterioration takes place. For the first time, however, the high-current field-effect transistor (FET) allows nearly ideal switch performance at low cost. Two types of switches are used in the analog generator: one type for linearly carrying low-power computation signals, and a second type for carrying large bursts of current to provide for initial capacitor charge.

The generator now in operation was designed before the high-current FET was available. It uses conventional transistors and diodes for the low-level signal switches, but has since been modified to utilize the superior characteristics of the FET for the high-current charging switches.

##### A. Diode Bridge for Conventional Signal Switching

Figure 7(a) shows the basic bridge circuit for switching low-level analog signals. By matching diodes, the signal offset voltage due to the trigger current which closes the switch can be made arbitrarily small. If diodes are operated in the linear region of their V-I characteristic (Fig. 8), the closed switch appears as a constant resistance in series with the operational amplifier of Fig. 7(b); removing the trigger current  $I$  opens the switch. The diodes carry a total current of  $I/2 \pm i/2$  (where  $i$  = signal current), with opposite arms of the bridge carrying equal currents.

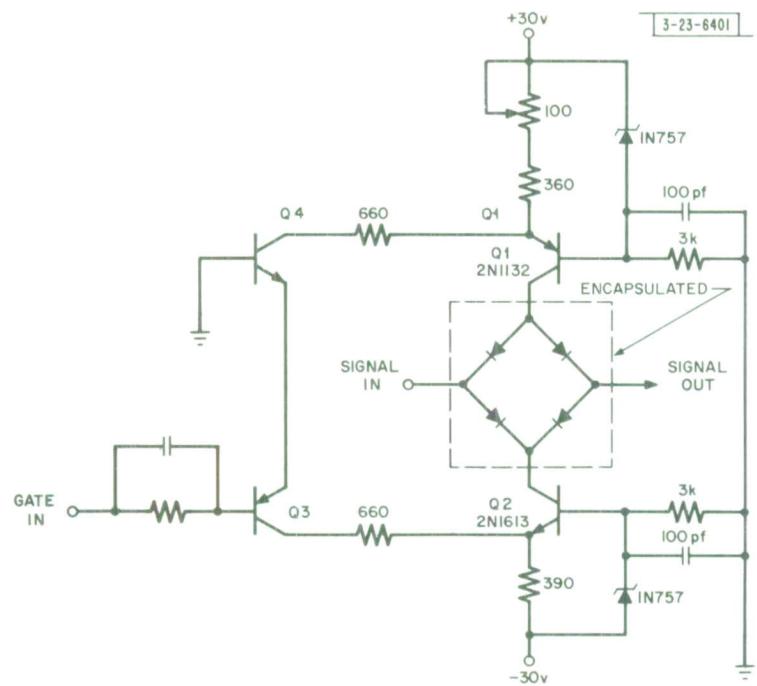


Fig. 9. Diode bridge and drive circuitry.

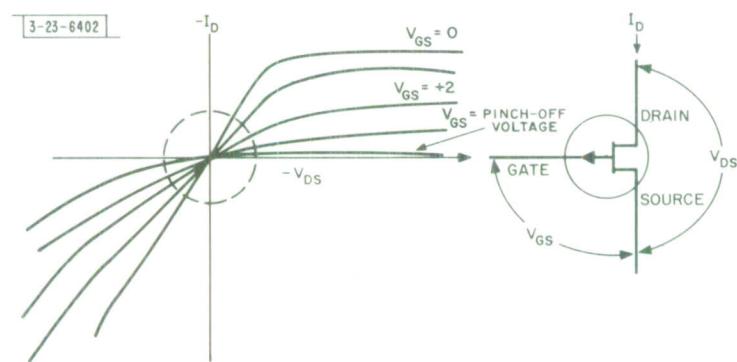


Fig. 10. FET characteristics.

Providing equal trigger currents in and out of the bridge is difficult unless the two trigger terminals can be isolated (e.g., by using a transformer). However, a DC switch is required, so the solution chosen was to locate the switch at the output of the operational amplifier as shown in Fig. 7(b). When this is done, any imbalance of trigger current will flow through the very low impedance of the operational amplifier rather than into the summing resistor. This reduces the imbalance current fed forward to a second-order effect resulting from the small voltage generated across the forward-biased diodes due to the imbalance current.

The penalty paid for this configuration is varying power through the trigger current source transistors, causing unequal heating and further current imbalance. Any current imbalance will cause a voltage offset in addition to the diode mismatch.

A driving circuit with two current sources, each using a transistor and zener-diode combination, was built to determine the magnitude of the voltage and current imbalance (Fig. 9). 1N903 diodes, which were selected for the bridge, exhibited a forward resistance of 10 ohms and were easily matched to 7-mv offset. Worst-case conditions of signal loading and heating gave a current imbalance of 0.6 ma. This accounted for a 3-mv offset through the 10-ohm forward-biased diodes, giving a total offset of 10 mv which fell within the 0.1-percent accuracy requirement.

Switching time increased for increasing load (summing) resistor values. To permit fast switching ( $2 \mu\text{sec}$ ) of larger summing resistors, the output of the diode bridge is shunted to ground with a 5-kohm resistor, decreasing the load on the switch to under 5 kohms. In the disabled state, the capacitance of the diode bridge (2 pf) can contribute to capacitance feedthrough during rapid input signal changes. The shunt resistance lowers the RC time constant and dumps large fractions of capacitance feedthrough current out of the computing path. Significant fractions of the bridge leakage currents ( $0.1 \mu\text{amp}$ ) are dumped out by the shunt resistance, giving excellent disabled gate characteristics.

The current source transistors Q1 and Q2 in Fig. 9 are switched off by dropping the emitter voltage below the base voltage held by the zeners. This occurs when Q3 is on, by turning on Q4, thereby steering current around Q1 and Q2. Once Q1 and Q2 are off, the diode-bridge trigger current goes to zero, turning off the analog switch. The main drawback of the switch is continual high-power consumption (approximately 2 watts) due to high biasing currents used in the bridge. For a large number of switches, this can become prohibitive.

## B. FET Switches

The FET version of the above switch not only performs better and runs much cooler, but is less expensive because much less circuitry is required for switch driving. Before the driving circuitry for the switch is discussed, however, FET characteristics should be understood.

The "on"-resistance is a minimum, typically 80 ohms, with zero  $V_{GS}$  (Fig. 10). With a  $V_{GS}$  equal to the pinch-off voltage, typically +7 volts for this application, the drain to source resistance is over 200 megohms, effectively turning the switch off. Notice the characteristics are symmetrical near the origin, resulting in bipolar operation at the same gain. The FET gate terminal behaves like a back-biased diode (shown schematically by the FET symbol in Fig. 10). Thus, the gate exhibits a high input impedance (for  $+V_{GS}$ ) typically over 200 megohms, passing only insignificant amounts of current into the signal path. For any one gate voltage, the resistance becomes increasingly nonlinear away from the origin. For proper analog switch operation, the "on"-resistance must be kept constant (within some acceptable error) over the expected operating ranges. Thus, a high-current FET is desirable since the resistance near the origin becomes

more linear with higher current-carrying capability. In the switch applications discussed below, maximum signal current is 1 ma and the FET saturation current is nominally 30 ma.

### C. Low-Power Signal Switching

Figure 11 shows the environment and design of low-power FET switches. The operational amplifier maintains zero volts at the FET drain terminal. The precision input resistor  $R_p$  is always larger than 2 kohms and is driven by  $V_s$  between  $\pm 10$  volts. Since the "on"-resistance of the FET is less than 100 ohms, the voltage appearing at the FET source is always between  $\pm 0.5$  volt in the "on" condition. The FET is activated by turning on the transistor, thereby back-biasing diode D1. Since diode D2 is always back-biased for the "on" state, the FET and gate-to-source resistor are isolated from the drive circuitry, and the combination appears as a two-terminal device. With positive  $V_s$ , no current flows through the gate-to-source external resistor since the gate is back-biased. Therefore,  $V_{GS}$  is maintained at zero volts. For  $-V_s$ , the FET gate is forward-biased and begins to conduct through the external gate-to-source resistor. If the resistor is large enough, the parallel combination with the FET will cause an insignificant change in total equivalent resistance. However, if the external resistance is too large, slow switching results due to stray capacitances in the FET. For this application, a 4-kohm resistor allowed a suitable compromise for 2- $\mu$ sec switching. With negative  $V_s$ , the gate voltage never goes below  $-0.005$  volt relative to the drain (since the FET is symmetrical, here one can regard the drain as the source), thereby introducing only a minor reduction in the FET "on"-resistance compared to the "on"-resistance for zero  $V_{GS}$ . No voltage or current offset occurs through the switch, since the FET and external resistor comprise a two-terminal device.

To turn the switch off, the transistor is turned off; current is steered from the power source through D1, through the gate-to-source resistor, bypassing the FET and dumping out via D2. Through voltage division, +15 volts appears at the FET gate, turning the device off.  $R_p$  drains current in both the "on" and "off" states, maintaining nearly a constant load on  $V_s$ . Since the FET source terminal is nearly at a constant 1.7 volts when the switch is off, no capacitance feedthrough occurs as  $V_s$  varies. However, stray capacitance does cause energy leakage during switching. Presently this switching feedthrough borders on the unacceptable for 0.1-percent accuracy operation. Either FETs with lower stray capacitance will have to be developed, or an inexpensive compensation method will have to be devised. The switching feedthrough poses the

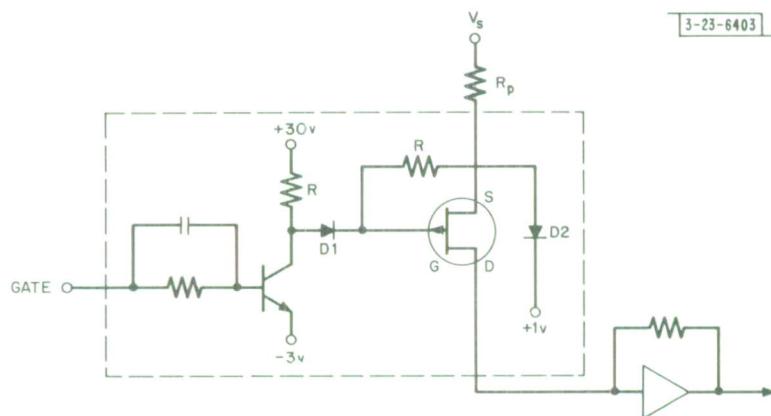


Fig. 11. FET analog switch and environment.

only problem in using this FET design as a switch. (However, this problem can be overcome by placing a modified version of the high-current switch (discussed below) at the operational amplifier output. Any capacitive feedthrough current will pass harmlessly into the low-impedance amplifier output rather than into the summing resistor. The only drawback of this approach is higher switch cost due to a higher component count.) Switch power drain is small, typically less than 300 mw, and no potentiometers are required. Only eight components are required, keeping fabrication cost low.

#### D. High-Current Switch

For charging the integrators, a switch was needed that could pass over 50 ma. Because charging is done differentially, and no current flows into the integrators when the charge is complete, the switch did not have to behave linearly as long as no offset was introduced at the end of the charging period. The FET switch discussed above was not suitable since the analog input resistor always drains current. In the charging application, nearly 50 ma could be drained when the above switch was off - clearly a waste of power.

The design shown in Fig. 12(a-b) was devised to meet the need for a switch capable of passing short bursts of current and drawing minimal current in the "off" condition.

Two FETs are placed in parallel to meet the 50-ma drain. In the "on" condition, the FETs are isolated from drive circuitry by the back-biased diode D1. Some signal current flows around the FETs to ground via the two shunt resistors R3 and R4, introducing permissible nonlinearities. When input signal voltage reaches zero, no current flows anywhere in the isolated FET assembly prohibiting any offset.

To turn the switch off, the transistor is turned off. The input voltage  $V_s$  is divided over  $R_1$ ,  $R_2$ ,  $R_3$  and  $R_4$  such that the voltage appearing at the FET gates is always greater than the FET pinch-off voltage (relative to the largest positive voltage at the drain or source), but not

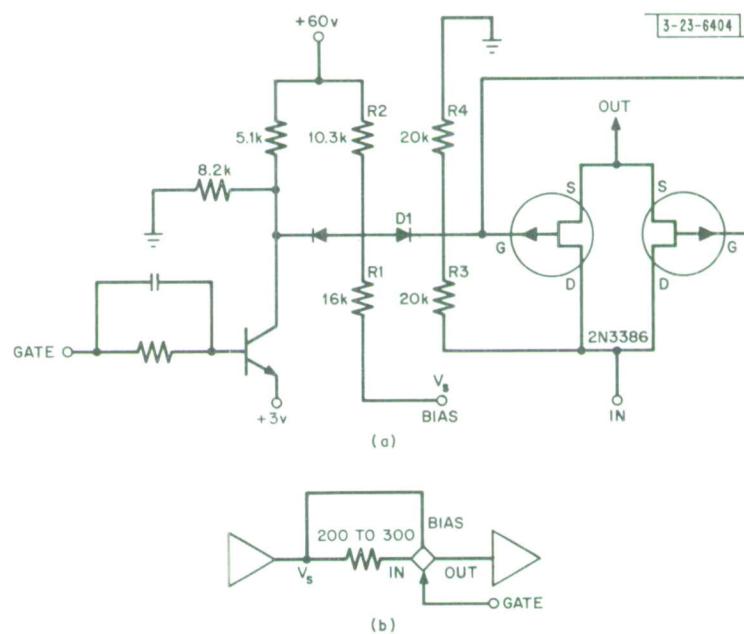


Fig. 12. (a) Current burst switch; (b) environment.

greater than the breakdown voltages of the FETs. This turns the FETs off and causes minimal current drain on  $V_S$ . The variable gate voltage is necessary since the FET drain voltage varies in the "off" condition. There is no clamping diode here as in the other FET design. The two shunt resistors around the FETs greatly reduce capacitive feedthrough during switching. Capacitive feedthrough in the signal paths is minimal since FET capacitance is reduced by large pinch-off voltages.

Note that the analog input resistor must, indeed, be small (typically 200 to 300 ohms) for proper switch operation. If it is too large, the pinch-off voltage could not be developed over the FET gate-to-drain resistor due to unbalancing of the voltage divider.

The cost of this switch is probably over double that of the low-power FET switch. However, only four high-power switches are used in the generator. Again, power consumption is low.

## V. PERFORMANCE AND COST

### A. Performance

Curves available	Point Line Parabola (rotated) Circle Hyperbola (orthogonal) Cubic (rotated)
Output	$\pm 3$ volts at $\pm 15$ ma (full scale)
Accuracy	0.1 percent of full scale
Repeatability	0.2 percent
Raster size	$1024 \times 1024$ div/viewable area
Point display time	40 $\mu$ sec
Random point display time (counting beam-settling time)	70 $\mu$ sec
Maximum curve deflection rate	6 volts/1 msec, or 1 raster unit/ $\mu$ sec
Initial condition charge (load) time	25 $\mu$ sec
Drift	None after $\frac{1}{2}$ hour warmup
Hold (storage) time of integrators to 0.1 percent	30 msec

The accuracy specification listed above unfortunately does not apply to small circles less than the size of nickel on a 10-in. raster - at maximum rate. These circles do not close. However, accurate small circles can be drawn by decreasing the initial rate below maximum. This sacrifices the feature of constant intensity regardless of radius and will cause brightening of the circle as smaller circles are drawn. The spiraling difficulty is due to stray capacitance in the D-A decoder switches. It is possible to compensate for this capacity, but this has not yet been attempted.

In the discussion on circles in Sec. II, it was shown that the reciprocal radius and its complement are placed in the X- and Y-registers for computation. If these numbers are not equal in magnitude, orthogonal ellipses should result. Actually, the spiraling difficulty is compounded, virtually eliminating the usefulness of this potential feature. However, ellipses can be approximated very accurately by four parametric cubic segments, and the orthogonal restriction no longer applies.

The curve displays are extremely sharp - no wiggles or noise can be seen on the traces. The 30-msec hold time might seem insufficient; however, when one remembers that over a hundred curves can be displayed in 30 msec, the hold time is easily sufficient. The hold feature is useful in drawing symbols. Here a start point is loaded and all subsequent lines of the symbol are formed by giving new rates, which turn the corners. Then, if the symbol is to be translated, the program furnishes a new start point and the rest takes care of itself; no further point calculations are necessary. Incidentally, the digital equivalent of the generator (the DDA) does have the advantage of infinite hold time since parameters are stored in flip-flops.

One disadvantage of analog assemblies is the large number of potentiometers required; this generator is no exception and has over fifty. The adjusting procedure is straightforward, although long and tedious. Once the potentiometers are aligned, they need not be touched again. The generator has been in daily operation (18 hours a day) for over three months without a potentiometer readjustment, and no drift has been noticed. Except for one connector failure, no other failures have occurred since the machine went on-line over five months ago.

### B. Cost

The inherent low cost of the analog generator, compared to its digital equivalent, can be appreciated by examining the computing and gating elements. The integrators are the analog equivalent of fully buffered, digital, incremental adder-subtractors. Since the generator operates at 0.1-percent accuracy, the digital equivalent must use 10 bits per register. To match the generator's speed, the ten flip-flops composing the digital adder-subtractor would have to operate at 4 Mcps. In addition, the digital register requires three to five logic elements per bit. Thus, the cost per bit (if built from discrete components) would be prohibitively high. Using integrated circuits, cost might be considerably lower, but this applies to the analog circuits as well.

The FET analog switch is also inherently less expensive than its digital equivalent. Since the FET passes signals accurate to 0.1 percent, it is equivalent to ten AND gates operating in parallel. The FET switch uses less than a sixth of the components required for the digital switch.

The present costs of components, only for the analog generator, break down as follows:

15 operational amplifiers at \$120 each	\$1800
50 FET switches at \$15 each	750
Precision components and potentiometers	<u>300</u>
	\$2850

Assembly costs are not included in the above.

Discussions of generators for scopes should include the cost of the digital control that decodes the commands from the driving digital computer. This cost can vary widely, since a control can be designed to run many generators simultaneously. Certain common features can be time-shared over many generators, thereby decreasing the cost per generator. The following comments apply to the cost of a control for a single generator.

The digital control is basically the same for either analog or digital generators, since the same parameters are loaded and switched identically. The control for an analog generator is slightly more expensive since adjustable digital delay units and associated gates are used to time out and to synchronize the various analog settling times. In a control for a digital generator, variable delay units are not necessary for timing since loading and switching take place in one clock cycle. In this particular design, six variable delays are used that do not occur in a DDA

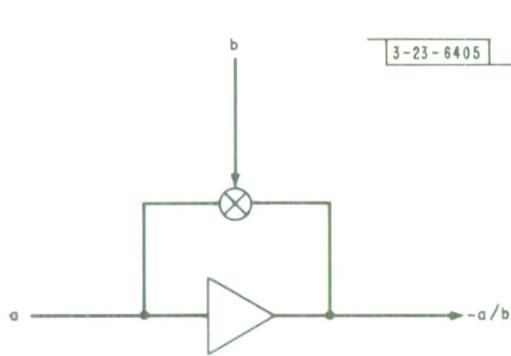


Fig. 13. Division using a multiplier and an operational amplifier.

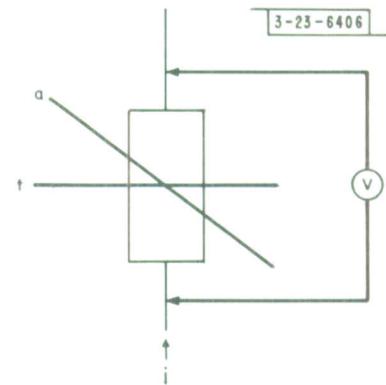


Fig. 14. Schematic of thin-film magnetoresistive multiplier.

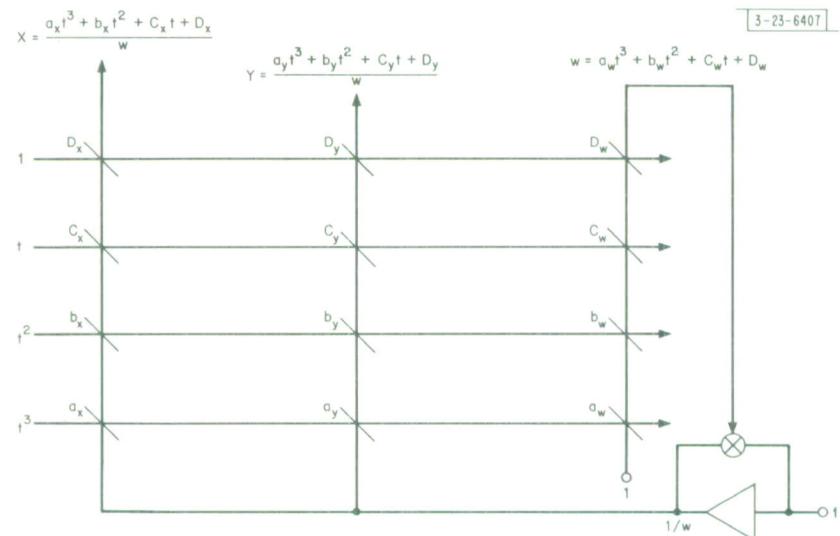


Fig. 15. Schematic of analog generator using thin-film multipliers.

control. A conservative estimate of \$5000 would cover parts and labor for the control unit. If integrated circuits were used, the price would probably be reduced sharply.

The total cost for generator and control unit can be spread over two or three scopes, if the generator is time-shared. (The generator would deflect all the scopes simultaneously, but only one of them would be intensified for any one curve.) At present, two scopes are being run from the existing generator with intensity controlled by command from the central computer.

## VI. THE FUTURE

Future display generators will assume even more of the computing tasks now done in the digital computer. The value of perspective drawing for some applications is being recognized, and generators capable of transforming a display into perspective will have to be built. This requires the introduction of dividers into the generator, since perspective transformations require division by the depth coordinate. A promising technique of performing division fast and accurately by analog techniques is being investigated at Lincoln Laboratory. The magneto-resistive effect of thin films is being studied for use as a high-speed multiplier. If this multiplier is placed in the feedback loop of an operational amplifier, division results as shown in Fig. 13.

The magnetoresistive multiplier is arranged so it can perform four-quadrant multiplication of three inputs. A schematic of this arrangement in Fig. 14 shows two inputs as horizontal and diagonal lines which represent fields equal to  $t$  and  $a$ . A third input  $i$  is a current flowing through the resistive element represented as a vertical bar. Output  $V$  is measured as a differential voltage over the resistive element equal to the product  $(a)(t)(i)$ . Dr. L. Roberts has suggested that these multipliers, which are merely thin-film deposits, be arranged as shown schematically in Fig. 15.

The two outputs  $X$  and  $Y$  are measured as differential voltages over the four series-resistive elements. Thus, the expensive differential amplifier can be amortized over four multipliers. With this arrangement, the same types of curves can be formed as with the analog generator discussed in this report. Furthermore, division is possible which permits not only perspective, but also formation of circles and ellipses. The device should properly be viewed as a matrix multiplier whose dimensions can be expanded in either direction without sacrificing accuracy.

With an analog matrix multiplier available, the scope generator can easily take on additional computation tasks, such as rotating 3-D objects without intervention of the directing digital computer, or perhaps even displaying entire surfaces.

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APPENDIX  
CRT DISPLAY DESIGN  
C. S. Lin

The design objective of the CRT display unit is to assure a medium-speed, good-quality display at a reasonable cost, that can be duplicated readily. Thus, the components used are mostly standard commercial parts.

The CRT is a rectangular, high-resolution, magnetic-deflection, electrostatic focusing television monitor tube, Sylvania 17DWP7. This tube is normally supplied with a P4 phosphor, but P7 was found to be more pleasing for this application. The CRT is mounted in a heavy magnetic shield which can be mounted directly in a 19-in. rack. The shield is made by the Perfection Mico Company under a part No. MS23895.

The CRT has deflection angles of 70° for the long axis and 50° for the short axis. Since only a square display is needed, 50° deflection is sufficient. The deflection yoke selected is a CELCO AY521-S 588, which requires  $\pm 2$  amp for a 52° deflection at 10 kv. The yoke is driven by a CELCO deflection driver DA-PP3 whose required power is  $\pm 20$  volts, regulated. A pair of Technipower M19.2, 6.0 amp supplies is used. The full-axis 52° deflection time for this configuration is approximately 65  $\mu$ sec.

Power supplies for the focusing, astigmatism controls and bias were constructed in-house, primarily to obtain a more compact unit. There is no special requirement other than that they should be well filtered and that the bias supply should be first to come on and last to go off. The intensification circuit is built into the supply. A -3-volt signal will intensify the CRT.

The post-acceleration voltage is 16 kv and is supplied by an unregulated Universal Voltronics BPE-16-1.5 supply. A regulated supply probably would improve the stability of the display somewhat.

A schematic of the CRT is shown in Fig. A-1.

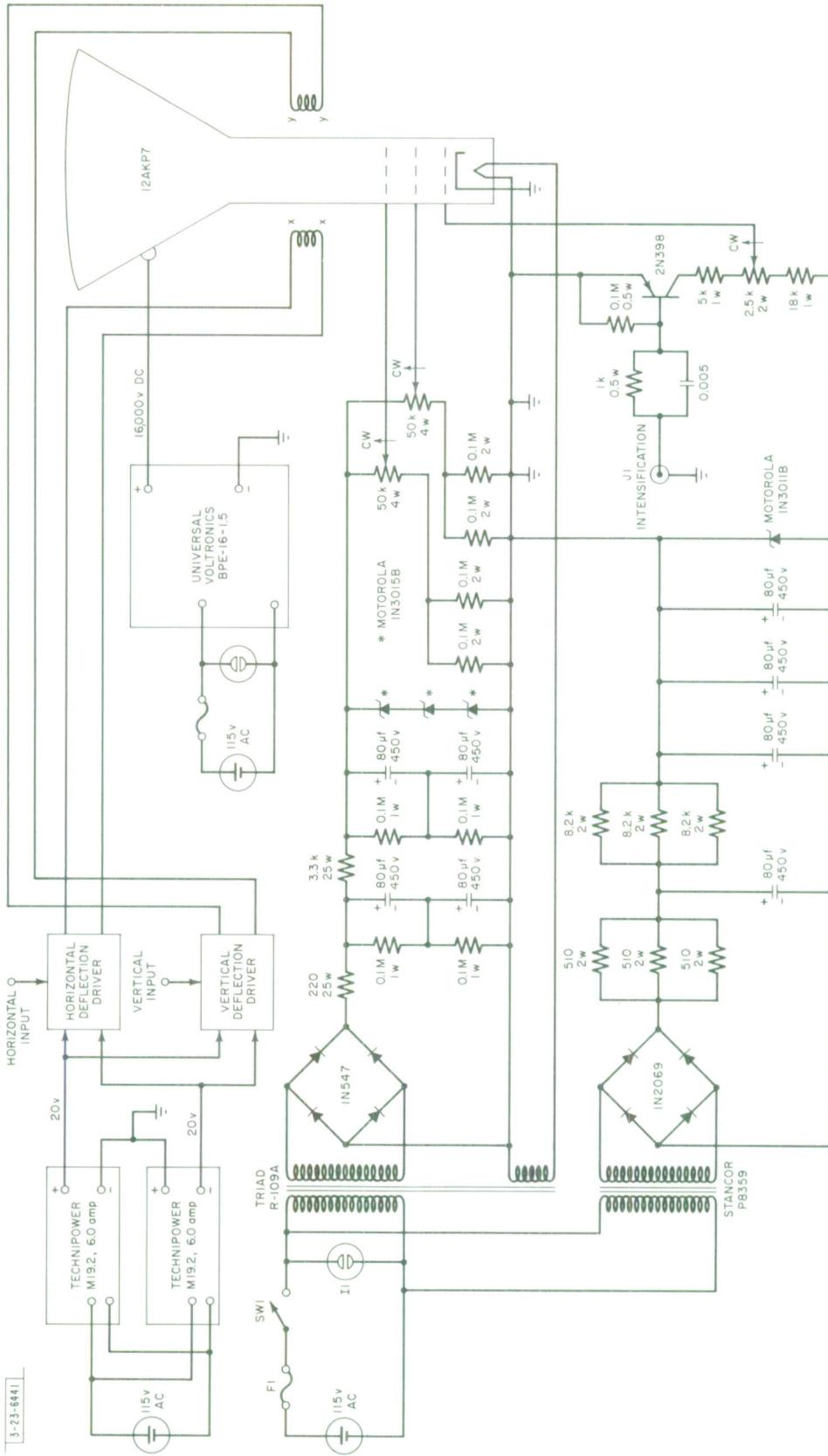


Fig. A-1. Schematic of CRT circuit.

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